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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/843,165	04/27/2001	Shinichi Kobayashi	57454-093	2071

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McDermott Will & Emery
600 13th Street NW
Washington, DC 20005

EXAMINER	
LE, VU ANH	
ART UNIT	PAPER NUMBER
2824	

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05/26/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/843,165	KOBAYASHI ET AL.	
	Examiner	Art Unit	
	Vu A. Le	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,3,5 and 6* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/043,889.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/13/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The written consent is missing. It is required a written consent being submitted in case the application is in condition for allowance, see MPEP § 1410.01 and 37 CFR 1.172(a)

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 2-3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yiu et al (***5,399,891***) in view of Montalvo et al (5,126,808).

1. With respect to claims 2 and 3, Yiu et al disclose a nonvolatile semiconductor memory device having all the claimed features such as a main bit line formed of metal wiring (global bit line 18 in Fig.1 and global BL is metal line, see col.10, lines 15-16); first and second subbit lines (first subbit line is the upper part of local bit line 11, second subbit line is the lower part of local bit line 11) connected in series and aligned parallel to said main bit line; first and second switching transistors (the block select transistor 21 in the upper and lower parts, see Fig.2), each responsive to a sector select signal

(TBSEL) for connecting said main bit line to a corresponding one of said first and second subbit lines; a first memory cell group (13…16 in the upper part, Fig.2) including n memory cells (n > 2), each connected to said first subbit line; a second memory cell group (13…16 in the lower part, Fig.2) including n memory cells, each connected to said second subbit line; wherein at least a part of the main bit line and at least a part of the subbit lines are formed in different layers (the global bit lines are in metal layer which is above the local bit line), each of said memory cells includes a control gate, a floating gate, a drain, and a source (see col.4, lines 45-59), and each of said memory cells is connected to a corresponding one of said first and second subbit lines via said drain (see col.4, lines 45-59); said device further comprising n connection lines (the middle part for connecting word line in the upper part and word line in the lower part, see Fig.2), each for connecting the control gate of a j-th memory cell j=I, 2,... n) in said first memory cell group located in a direction farther from said second memory cell group to the control gate of a j-th memory cell in said second memory cell group located in a direction farther from said first memory cell group; and row decoder means (104, Fig.3) responsive to an externally applied address signal for selecting one of said n connection lines.

2. Yiu et al fails to disclose or suggest the first and second subbit lines formed of metal wiring. However, Montalvo et al disclose a memory device (Fig.5) having first and second subbit line formed of metal wiring (see col.9, lines 59-66 and Fig.5). Thus, it would have been obvious to one of ordinary skill in the art at the time this invention was

made to modify Yiu et al by using metal wiring as first and second subbit line such as taught by Montalvo et al in order to increase the operation speed of the memory device.

With respect to claim 5, Yiu et al disclose a nonvolatile semiconductor memory device having all the claimed features such as a first bit line formed of metal wiring (global bit line 18 in Fig.1 and global BL is metal line, see col.10, lines 15-16); a switch (the block select transistor 2, see Fig.2) having a conductive end connected to said first bit line; a second bit line (local bit line 11, Fig.1) connected to other conductive end of said switch; a plurality of memory cells (13-16, Fig.1) connected to said second bit line, each including a drain, a control gate, a floating gate and a source (see col.4, lines 45-59); and a source line formed with an active laver (see col.7, lines 59-64), to which said sources of said memory cells are commonly connected, wherein at least a part of the first bit line and at least a part of the second bit line are formed in different layers (the local bit line and main bit line of Yiu et al are in buried diffusion layer and metal layer).

Yiu et al fails to disclose or suggest the second subbit line formed of metal wiring. However, Montalvo et al disclose a memory device (Fig.5) having the second subbit line formed of metal wiring (see col.9, lines 59-66 and Fig.5). Thus, it would have been obvious to one of ordinary skill in the art at the time this invention was made to modify Yiu et al by using metal wiring as the second subbit line such as taught by Montalvo et al in order to increase the operation speed of the memory device.

3. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yiu et al (***5,399,891***) in view of Yasuda et al (5,260,899).

Yiu et al disclose a nonvolatile semiconductor memory device having all the claimed features such as a first bit line formed of metal wiring (global bit line 18 in Fig.1 and global BL is metal line, see col.10, lines 15-16); a switch (the block select transistor 2, see Fig.2) having a conductive end connected to said first bit line; a second bit line (local bit line 11, Fig.1) connected to other conductive end of said switch; a plurality of memory cells (13-16, Fig.1) connected to said second bit line, each including a drain, a control gate, a floating gate and a source (see col.4, lines 45-59); and a source line formed with an active laver (see col.7, lines 59-64), to which said sources of said memory cells are commonly connected.

Yiu et al fails to disclose or suggest the second bit line formed of polycrystalline silicon. However, Yasuda et al teach bit line is formed of polycrystalline silicon (col.7, lines 45-68 and col.12, lines 1-4)). Thus, it would have been obvious to one of ordinary skill in the art at the time this invention was made to modify Yiu et al by using second bit line formed of polycrystalline silicon such as taught by Yasuda et al to reduce the bit line stray capacitance.

Allowable Subject Matter

4. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: claim 4 recites said ***n connection lines are formed of polycrystalline silicon***, and ***wiring for connection between said row decoder and said n connecting lines is formed of metal wiring*** which is not disclosed or suggested by the PRIOR ART.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vu A. Le whose telephone number is (571) 272-1871. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Vu A. Le/

Primary Examiner, Art Unit 2824

Vu A. Le
Primary Examiner
Art Unit 2824

05/21/2009